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August 29, 2002

WRITER'S DIRECT NUMBER: (202) 218-7831

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Re:

Commissioner for Patents Washington, D.C. 20231

U.S. Utility Patent Application

Appl. No. 10/020,207; Filed: December 18, 2001

Ball Grid Array Package Substrates and Method of Making the Same

Inventors:

Khan et al.

Our Ref:

1875.1640000

Sir:

Transmitted herewith for appropriate action are the following documents:

- Information Disclosure Statement (IDS); 1.
- A listing of the cited documents on Form PTO-1449 (20 pages); 2.
- Copies of the one hundred five (105) documents listed on the PTO Form-1449; 3. and
- 4. One (1) return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

Commissioner for Patents August 29, 2002 Page 2

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jeffrey S. Weaver

Attorney for Applicants

July S. Wia

Registration No. 45,608

JSW/adw Enclosures

SKGF_DC1:50172.1





IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Khan et al.

Appl. No. 10/020,207

Filed: December 18, 2001

For: Bal

Ball Grid Array Package

Substrates and Method of Making

the Same

Confirmation No. 7969

Art Unit: 2811

Examiner: To be assigned

Atty. Docket: 1875.1640000

Information Disclosure Statement

Commissioner for Patents Washington, D.C. 20231

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Where the publication date of a listed document does not provide a month of publication, the year of publication of the listed document is sufficiently earlier than the effective U.S. filing date and any foreign priority date so that the month of publication is not in issue. Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.



This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

- 1. This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.
- □ 2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.
 - □ a. I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
 - □ b. I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

	□ c.	Attached is our Check No in the amount of \$ in payment
		of the fee under 37 C.F.R. § 1.17(p).
□ 3.	This I	information Disclosure Statement is being filed more than three months after
		the U.S. filing date and after the mailing date of a Final Rejection or Notice
		of Allowance, but before payment of the Issue Fee. Enclosed find our Check
		No in the amount of \$ in payment of the fee under 37
		C.F.R. § 1.17(p); in addition:
	□ a.	I hereby state that each item of information contained in this Information
		Disclosure Statement was cited in a communication from a foreign
		patent office in a counterpart foreign application not more than three
		months prior to the filing of this Information Disclosure Statement.
		37 C.F.R. § 1.97(e)(1).
	□ b.	I hereby state that no item of information in this Information Disclosure
		Statement was cited in a communication from a foreign patent office
		in a counterpart foreign application and, to my knowledge after
		making reasonable inquiry, was known to any individual designated
		in 37 C.F.R. § 1.56(c) more than three months prior to the filing of
		this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
□ 4.	The d	ocument(s) was/were cited in a search report by a foreign patent office in a
		counterpart foreign application. Submission of an English language version
		of the search report that indicates the degree of relevance found by the
		foreign office is provided in satisfaction of the requirement for a concise
		explanation of relevance. 1138 OG 37, 38.
□ 5.	A cor	ncise explanation of the relevance of the non-English language document(s)
		appears below:
□ 6.	Copie	es of the documents were cited by or submitted to the Office in an IDS that
		complies with 37 C.F.R. § 1.98(a)-(c) in Application No, filed
		, which is relied upon for an earlier filing date under 35 U.S.C.
		§ 120. Thus, copies of these documents are not attached. 37 C.F.R.
		§ 1.98(d).



It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Ur S. Wer

Jeffrey S. Weaver

Attorney for Applicants Registration No. 45,608

Date: 8-29-02

1100 New York Avenue, N.W. Suite 600 Washington, D.C. 20005-3934 (202) 371-2600

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT PRADEM

ATTY. DOCKET NO. 1875.1640000

APPLICATION NO. 10/020,207

APPLICANT Khan et al.

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	AO	1		Amkor Electronics, "Amkor BGA Packaging: Taking The World By Storm", Electronic Packaging & Production, Cahners Publishing Company, May 1994, page unknown.									
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	AQ	1					d Array Technology is, 10 pages.	," Ball Grid	Array	National S	mposium,		
	AR	1	Attarwala, A.I. Dr. and Stierman, R., "Failure Mode Analysis of a 540 Pin Plastic Ball Grid Array", Surface Mount International Conference, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 252-257.										
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		l	OTHER (Including Author, Title, Date, Pertinent Pages, etc.)									
	AN	<u>2</u>	Banerji, K., "Development of the Slightly Larger Than IC Carrier (SLICC), Journal of Surface Mount Technology, July 1994, pp. 21-26.									
	AO	2	Bauer, C., I Journal of	Ph.D., Surfac	, "Partition ce Mount 1	ing aı Fechn	nd Die Selection Strate ology, October 1994, p	gies for Cos op. 4-9.	: Effective Mo	CM Designs",		
	AP	<u>2</u>	Component	ts". Si	urface Mou	unt In	P: A Summary of Tracternational Conference observed in 1994, San Jose,	e Proceedina	s, Surface M	ount		
	AQ	<u>2</u>	Burgos, J. et al., "Achieving Accurate Thermal Characterization Using a CFD Code A Case Study of Plastic Packages", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part A, IEEE, December 1995, Vol. 18, No. 4, pp. 732-738.									
	AR	<u>2</u>	Chadima, M., "Interconnecting Structure Manufacturing Technology," Ball Grid Array Natio Symposium, Dallas, Texas, March 29-30, 1995.									
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in

conformance and not considered. Include copy of this form with next communication to Applicant.

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	AN	<u>3</u>	Chanchani P. et al. "Mini RGA: Pad and Pitch Face Die Test and Handling". Advanced										
	AO	3	Chung, T.0 Array Natio	C. et a onal S	l., "Reworl ymposium	k of P Proc	lastic, Ceramic, and eedings, Dallas, Tex	Tape Ball as, March	Grid A 29-30,	rray Assem 1995, pp.	iblies", Ball Grid 1-15.		
	AP	<u>3</u>	Cole, M.S. Surface Me 4-11.	and C ount T	aulfield, T echnology	. "A R , Suri	eview of Available E face Mount Technol	Ball Grid A ogy Assoc	rray (B iation,	GA) Packad January 19	ges", Journal of 96, Vol. 9, pp.		
	AQ	<u>3</u>	Cole, M.S. Conferenc California,	and C e Proc pp. 14	aulfield, T eedings, S 17-153.	., "Ba urfac	ll Grid Array Packag e Mount Internation	ing", Surfa nal, August	ace Mo t 28-Se	unt Interna ptember1,	itional 1994, San Jose,		
	AR	<u>3</u>	Dobers, M Advanced and 32.	. and : Packa	Seyffert, M ging, IHS	1., "Lo Publis	ow Cost MCMs: BGA hing Group, Septem	s Provide nber/Octol	a Fine- per 199	Pitch Alterr 14, Vol. 3, N	native", No. 5, pp. 28, 30		
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ATTY. DOCKET NO. 1875.1640000	APPLICATION NO. 10/020,207
APPLICANT Khan et al.	
FILING DATE December 18, 2001	GROUP 2811

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	AO	<u>4</u>	Edwards, D. et al., "The Effect of Internal Package Delaminations on the Thermal Performance of PQFP, Thermally Enhanced PQFP, LOC and BGA Packages", 45th Electronic Components & Technology Conference, IEEE, May 21-24, 1995, Las Vegas, NV, pp. 285-292.									
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INFORMATION DISCLOSURE STATEMENT

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ATTY. DOCKET NO. 1875.1640000	APPLICATION NO. 10/020,207
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FILING DATE December 18., 2001	GROUP 2811

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	AO	<u>5</u>	Ferguson, l No. 2, pp. !	M. "Eı 54, 56	nsuring Hig 5 and 58.	jh-Yi€	eld BGA Assembly",	Circuits	s Assembly	, February	1995, Vol. 6,
	AP	<u>5</u>	Freda, M., Cahners Pu	"Lami ıblishi	nate Techi ng Compa	nolog ny, O	y for IC Packaging' ctober 1995, Vol. 3	', Electr 5, No. :	onic Packa 11, pp. S4	aging & Pro -S5.	duction,
	Freedman, M., "Package Size and Pin-Out Standardization", Ball Grid Array National Symposium, March 29-30, 1995, 7 pages.										onal
	AR	<u>5</u>	Freyman, E High Interd Electronic (3. and connection compo	Pennisi, R ct Density onents & T	, "O IC Pa echn	ver-molded Plastic l ckaging Solution fo ology Conference,	Pad Arra or Consu IEEE, M	ary Carrier umer and I lay 11-16,	s (OMPAC) Industrial E 1991, pp. :	: A Low Cost, lectronics", 41st 176-82.
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INFORMATION DISCLOSURE STATEMENT

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	AN	<u>6</u>	Freyman, B. Mount Inter	et al	I., "Surface	Mou ence	nt Process Technology fo Proceedings, Surface Mo alifornia, pp. 81-85.	·	l Array Packa ational, Augu	iging", Surface ust 29-			
	AO	19	Freyman, B. Conference	et al Proce	., "The Mo eedings, Sa	ve to	Perimeter Plastic BGAs" se, CA, August 29-31, 19	, Surface N 195, pp. 37	1ount Interna 3-382.	ational			
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	AQ	<u>6</u>	Gilleo, K., "E IHS Publishi	Gilleo, K., "Electronic Polymers: Die Attach and Oriented Z-Axis Films", Advanced Packaging, IHS Publishing Group, September/October 1994, Vol. 3, No. 5, pp. 37-38, 40 and 42.									
	AR	<u>6</u>	Guenin, B. e Transactions Components 4, pp. 749-7	s on C s, Pac	"Analysis o Component kaging, an	of a T ts, Pa Id Ma	hermally Enhanced Ball ckaging, and Manufactu nufacturing Technology	Grid Array ring Techn Society, De	Package", IE ology, Part A ecember 199	EE , IEEE 5, Vol. 18, No.			
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ATTY. DOCKET NO. 1875.1640000	APPLICATION NO. 10/020,207
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	AN	7	Hart, C., "V Conference California, p	Hart, C., "Vias in Pads for Coarse and Fine Pitch Ball Grid Arrays", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 203-207.							
	АО	7	Hart, C. "Vi	Hart, C. "Vias in Pads", Circuits Assembly, February 1995, Vol. 6, No. 2, pp. 42, 44-46 and 50.							
	АР	7	Hattas, D., Technology 3, pp. 44-4	Hattas, D., "BGAs Face Production Testing: New Package Offers Promise but Must Clear Technology Hurdles.", Advanced Packaging, IHS Publishing Group, Summer 1993, Vol. 2, No. 3, pp. 44-46.							
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	AR	7	Hodson, T., unknown.	"Stu	dy Examin	es BO	6A Use", Electronic I	Packagin	g & Prod	uction, Ma	rch 1993, page
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	AN	<u>8</u>	Holden, H., Interconne Diego, CA,	, "The cting Janua	Many Tec and Packa ary 18-19,	hniqu ging 1 1996	ues of Small Via Form Electronic Circuits Bal , pp. 1-7.	nation fo II Grid Ar	r Thin B ray Nat	oạrds", The ional Symp	e Institute for osium, San
	AO	<u>8</u>	Houghten, Winter 199	Houghten, J., "New Package Takes On QFPs", Advanced Packaging, IHS Publishing Group, Winter 1993, Vol. 2, No. 1, pp. 38-39.							
	AP	<u>8</u>	"How To Give Your BGAs A Better Bottom Line.", Advanced Packaging, IHS Publishing Group, January/February 1995, page unknown.								
	AQ	<u>8</u>	Huang, W. by Simulati West '95, F	Huang, W. and Ricks, J., "Electrical Characterization of PBGA for Communication Applications by Simulation and Measurement", National Electronic Packaging and Production Conference West '95, February 26-March 2, 1995, Anaheim, California, pp. 300-307.							
	AR	8	Hundt, M. e and Produc 29, 1996, p	tion (onference	Enha Wes	ncements of Ball Grid t '95, Reed Exhibition	l Arrays" Compa	, Nation nies, An	al Electron aheim, CA,	ic Packaging February 25-
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	AN	9	Hutchins, (Publishing	Hutchins, C.L., "Understanding Grid Array Packages", Surface Mount Technology Magazine, IHS Publishing Group, November 1994, Vol. 8, No. 11, pp. 12-13.							
	AO	9	Hwang, J.S IHS Publish	Hwang, J.S., "Reliability of BGA Solder Interconnections", Surface Mount Technology Magazine, HS Publishing Group, September 1994, Vol. 8, No. 9, pp. 14-15.							
	AP	9	Hwang, J.S IHS Publish	Hwang, J.S., "A Hybrid of QFP and BGA Architectures", Surface Mount Technology Magazine, IHS Publishing Group, February 1995, Vol. 9, No. 2, p. 18.							
	AQ	9	Johnson, R Packaging 413-422.	Johnson, R. et al., "A Feasibility Study of of Ball Grid Array Packaging", National Electronic Packaging and Production Conference East '93, Boston, Massachusetts, June 14-17, 1993, pp. 413-422.							
	AR	9	Johnson, R National El 14-17, 199	ectron	ic Packagir	ıl Cha ng &	racterization of 140 Production Conferen	and 22 nce Eas	25 Pin Ball et '93, Bos	Grid Array ton, Massa	Packages", chusetts, June
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	AN	<u>10</u>	Johnston, Dallas, Te	P., "L xas, M	and Patter larch 29-30	n Inte 0, 199	erconnectivity Schen 15, pages 2-21.	nes",	Ball Grid Ar	ray Nationa	ıl Symposium,
	AO	<u>10</u>	Johnston, Surface M 12-18.	ohnston, P. "Printed Circuit Board Design Guidelines for Ball Grid Array Packages", Journal of Surface Mount Technology, Surface Mount Technology Association, January 1996, Vol. 9, pp. 2-18.							
	АР	<u>10</u>	Kawahara Proceedin Septembe	, T. et gs of t r 24-2	al., "Ball (he 1995 II 7, 1995, p	Grid A nterna p. 57	rray Type Package I Itional Electronics Pa 7-587.	By Us ackag	ing of New ing Confere	Encapsulat ence, San D	ion Method", iego, CA,
	AQ	<u>10</u>	Knickerbo Packaging	Knickerbocker, J.U. and Cole, M.S., "Ceramic BGA: A Packaging Alternative", Advanced Packaging, IHS Publishing Group, January/February 1995, Vol. 4, No. 1, pp. 20, 22 and 25.						dvanced , 22 and 25.	
	AR	<u>10</u>	Kromann, Microproc February	G., et essor" 26-Ma	al., "A Hi- , National rch 2, 199	Densi Electr 5, Ana	ty C4/CBGA Interco onic Packaging and sheim, California, pp	nnect Produ D. 152	Technology uction Confe 3-1529.	y for a CMC erence Wes	OS et '95, IEEE,
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	AN	<u>11</u>	Kunkle, R., Texas, Marc	"Disc	rete Wiring -30, 1995,	g for A	Array Packages", B ges.	all Grid /	Array Nati	onal Symp	osium, Dallas,
	AO	11	Lall, B. et a Component 18, No. 4, p	s, Pa	ckaging, ai	for T nd Ma	hermal Evaluation Inufacturing Techn	of Multio	chip Modu art A, IEEE	ıles", IEEE E, Decembe	Transactions on er 1995, Vol.
	АР	<u>11</u>	Lasance, C. Independer Manufactur Technology	et al nt Cor ing T Soci	., "Therma npact Mod echnology ety, Decen	l Cha lels", Part in nber 1	racterization of Ele IEEE Transactions A, IEEE Componen 1995, Vol. 18, No.	ectronic [on Comp ts, Packa 4, pp. 72	Devices working the policy of	ith Bounda Packaging, I Manufact	ry Condition and uring
	AQ	11	Lau, J., "Ba	II Grid	d Array Teo	chnok	ogy", McGraw-Hill I	Inc., 199	95, entire	book subm	itted.
	AR	<u>11</u>	Lau, J. et al Wela Public	., "No ation	o Clean Ma s Ltd., Vol.	iss Re . 20, f	flow of Large Plast No. 3, March 1994,	ic Ball G pp.15-2	rid Array 22.	Packages",	Circuit World,
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	AN	<u>12</u>	"Literature Cahners Pu	Revie blicat	ew", Specia ion, 10 pag	al Sup ges.	plement to Electron	ic Packaging	& Pro	oduction,	February 1995,
	AO	<u>12</u>	LSI LOGIC document s	SI LOGIC Package Selector Guide, Second Edition, LSI Logic Corporation, 1994-1995, entire locument submitted.							
	АР	<u>12</u>	"LTCC MCM September/	s Lea Octo	nd to Ceran ber 1994, '	nic B(Vol. 3	GAs," Advanced Pac , No. 5, pp. 14-15.	kaging, IHS I	Publis	hing Grou	ıp,
	AQ	<u>12</u>	Mak, Dr. W Finite Eleme October 199	.C. et ent M 94, p	al., "Incre lodeling", J p. 33-41.	eased lourna	SOIC Power Dissipa al of Surface Mount	ation Capabili Technology,	ty Thi Surfa	rough Boa ice Mount	ard Design and International,
	AR	<u>12</u>	Marrs, R.C. Advanced P 50, and 52.	and (Olachea, G ging, IHS F	i., "BC Publis	SAs For MCMs: Char hing Group, Septem	nging Markets ber/October	s and 1994	Product i , Vol. 3, N	Functionality", No. 5, pp. 48,
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	AN	<u>13</u>	Matthew, L Packaging,	.C. et IHS F	al., "Area Publishing	Array Group	/ Packaging: KGD in o, July/August 1994	a Chip-S , pp. 91-9	ized Pac 94.	kage", Adv	ranced
	AO	<u>13</u>	I Internation	atthew, L.C. et al., "Area Array Packaging: KGD in a Chip-Sized Package", Advanced ackaging, IHS Publishing Group, July/August 1994, pp. 91-94. awer, A. et al., "Plastic BGA Solder Joint Reliability Considerations", Surface Mount ternational Conference Proceedings, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 239-251.							
	АР	<u>13</u>	Mazzullo, T Technology	. and Mag	Schaertl, l azine, Feb	L., "H ruary	ow IC Packages Affo 1995, Vol. 9, No. 2	ect PCB D	Design", : -116.	Surface Mo	ount
	AQ	<u>13</u>	Mearig, J., and Produc 295-299.	"An C tion (overview of Conference	f Man e Wes	ufacturing BGA Tec t '95, February 26-N	hnology", March 2, 1	, Nationa 1995, An	al Electroni aheim, Ca	c Packaging lifornia, pp.
	AR	<u>13</u>	Mertol, A., Grid Array I Technology	"Appl Packa Part	ication of t ges", IEEE B: Advan	the Tar Tran	aguchi Method on the sactions on Componackaging, IEEE, Nov	ne Robust nents, Pac vember 19	Design ckaging, 995, Vol	of Molded and Manu . 18, No. 4	225 Plastic Ball facturing , pp. 734-743.

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	AN	14 l	Array Com	poner	its", Surfac	e Mo	Practical Comparison unt International Co ber1, 1994, San Jo	nferenc	e Procee	dinas, Surfa	/ for Ball Grid ace Mount
	AO	14	Mulgaonker, S. et al., "An Assessment of the Thermal Performance of the PBGA Family' Eleventh Annual IEEE Semiconductor Thermal Measurement and Management Symposi IEEE, San Jose, CA, February 7-9, 1995,pp. 17-27.							Family", Symposium,	
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	AQ	14	Olachea, G Production	., "Ma (Spec	naging He cial Supple	eat: A ment	Focus on Power IC , Cahners Publishin	Packag g Compa	ing", Elec any, Nove	tronic Pack ember 1994	kaging & 1, pp. 26-28.
	AR	14	"Pad Array Company,	Impro May 1	oves Densi .992, pp. 2	ty", E 5-26.	lectronic Packaging	& Produ	uction, Ca	ahners Publ	ishing
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	AN	<u>15</u>	Partridge, J Journal of S 15-20.	. and Surfac	Viswanad e Mount T	ham, echn	P., "Organic Carrier ology, Surface Moui	Requ	uirements fo chnology As:	r Flip Chip sociation, J	Assemblies", uly 1994, pp.		
	AO	<u>15</u>	Ramirez, C. Array", Sur August 28-	Ramirez, C. and Fauser, S., "Fatigue Life Comparison of The Perimeter and Full Plastic Ball Grid Array", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 258-266.									
	АР	<u>15</u>	Rogren, P., "MCM-L Built on Ball Grid Array Formats", National Electronic Packaging and Production Conference West '94, Anaheim, California, pp. 1277-1282.										
	AQ	<u>15</u>	Rooks, S., ' Internation California, p	'X-Ra al, Pro op. 19	y Inspection oceedings 95-202.	on of of Th	Flip Chip Attach Usi e Technical Progran	ng Di n, Au	gital Tomosy gust 28-Sep	nthesis", Stember1, 1	Surface Mount 994, San Jose,		
	AR	<u>15</u>	Rukavina, J Symposium	., "At , Dall	tachment as, Texas,	Metho Marc	odologies: Ball Grid h 29-30, 1995, 37 p	Array	Technology	", Ball Grid	Array National		
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	Sack, T., "Inspection Technology", Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995, pages 1-41.												
	AO	Sakaguchi, H., "BGA MountingTechnology," pgs. 1-4, date and source unknown.											
	АР	<u>16</u>	Schmolze, C Packaging 8	and Prod	Fraser, A. Juction, Ja	, "SP: nuary	ICE Modeling Helps 1995, pp. 50-52.	Enha	nce BGA Pe	erformance"	, Electronic		
	AQ	<u>16</u>	Semiconductor Group Package Outlines Reference Guide, Texas Instruments, 1995, entire document submitted.										
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	AN	<u>17</u>	Sigliano, R. Advanced P	, "Usi ackag	ng BGA Pa ging, IHS F	ckage Publis	es: An Appealing Tech hing Group, March/Api	nolog ril 199	y in a QFP 94, pp. 36-	and Fine- 39.	Pitch Market",
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	AR	<u>17</u>	Tuck, J., "B 24, 26, and	GA To 28.	echnology	Brand	ches Out", Circuits Ass	embly	y, Februar	y 1995, Va	l. 6, No. 2, pp.
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	AN	<u>18</u>	"Tutorial and Short Courses", 45th Electronic Components & Technology Conference, May 21-24, 1995, Las Vegas, Nevada, IEEE, 6 pages.												
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